

# 74LVT240

3.3 V Octal inverting buffer/line driver; 3-state

Rev. 4 — 28 July 2021

Product data sheet

## 1. General description

The 74LVT240 is an 8-bit inverting buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables ( $1\bar{OE}$  and  $2\bar{OE}$ ), each controlling four of the 3-state outputs. A HIGH on  $n\bar{OE}$  causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs.

## 2. Features and benefits

- Octal bus interface
- 3-state buffers
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Output capability: +64 mA and -32 mA
- Direct interface with TTL levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74LVT240D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm		SOT163-1
74LVT240PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm		SOT360-1

## 4. Functional diagram

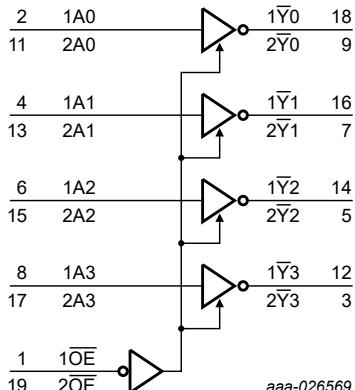


Fig. 1. Logic symbol

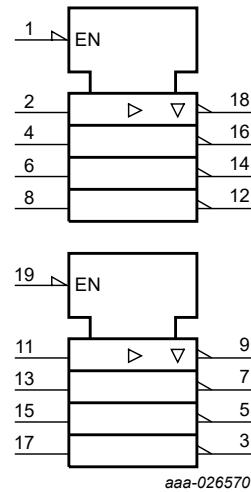


Fig. 2. IEC logic symbol

## 5. Pinning information

### 5.1. Pinning

74LVT240

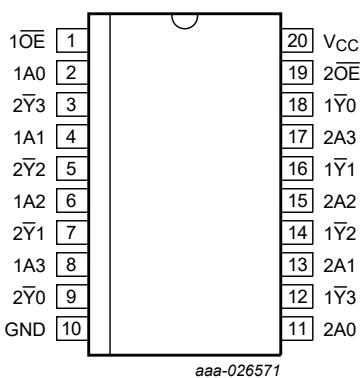


Fig. 3. Pin configuration SOT163-1 (SO20)

74LVT240

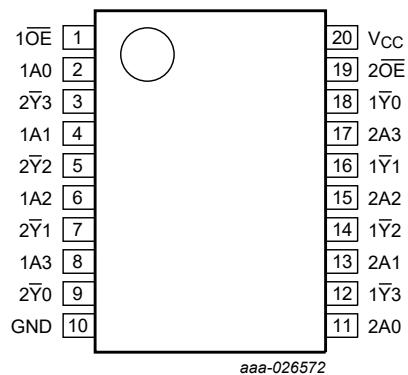


Fig. 4. Pin configuration SOT360-1 (TSSOP20)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	bus output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	bus output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Inputs		Outputs
nOE	nAn	nYn
L	L	H
L	H	L
H	X	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V	
V <sub>I</sub>	input voltage		[1]	-0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF or HIGH state	[1]	-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA	
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA	
I <sub>O</sub>	output current	output in LOW state	-	128	mA	
		output in HIGH state	-64	-	mA	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
T <sub>j</sub>	junction temperature		[2]	-	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C	-	500	mW	

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		2.7	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
I <sub>OH</sub>	HIGH-level output current		-32	-	mA
I <sub>OL</sub>	LOW-level output current		-	32	mA
		current duty cycle ≤ 50 %; f <sub>i</sub> ≥ 1 kHz	-	64	mA
T <sub>amb</sub>	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 2.7 V; I <sub>IK</sub> = -18 mA	-1.2	-0.9	-	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 2.7 V to 3.6 V; I <sub>OH</sub> = -100 µA	V <sub>CC</sub> - 0.2	V <sub>CC</sub> - 0.1	-	V
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -8 mA	2.4	2.5	-	V
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -32 mA	2.0	2.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 100 µA		0.1	0.2	V
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 24 mA	-	0.3	0.5	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA	-	0.25	0.4	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 32 mA	-	0.3	0.5	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 64 mA	-	0.4	0.55	V
I <sub>I</sub>	input leakage current	all input pins				
		V <sub>CC</sub> = 0 V or 3.6 V; V <sub>I</sub> = 5.5 V	-	1	10	µA
		control pins				
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	±0.1	±1	µA
		data pins	[2]			
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub>		0.1	1	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.5 V	-	1	±100	µA
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 0.8 V	75	150	-	µA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 2.0 V	-	-150	-75	µA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V to 3.6 V	[3]	500	-	µA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V to 3.6 V		-	-	-500 µA
I <sub>CEX</sub>	output high leakage current	n <sub>Y</sub> n output in HIGH-state when V <sub>O</sub> > V <sub>CC</sub> ; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 3.0 V	-	60	125	µA
I <sub>O(pu/pd)</sub>	power-up/power-down output current	V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; n <sub>OE</sub> = don't care	[4]	-	±1	±100 µA
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 3.0 V		1	5	µA
		V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 0.5 V		-5	-1	- µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A				
		outputs HIGH	-	0.12	0.19	mA
		outputs LOW	-	3	12	mA
		outputs disabled	[5]	-	0.12	0.19 mA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; one input = V <sub>CC</sub> - 0.6 V; other inputs at V <sub>CC</sub> or GND		-	0.1	0.2 mA

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or 3.0 V	-	4	-	pF
C <sub>O</sub>	output capacitance	outputs disabled; V <sub>O</sub> = 0 V or 3.0 V	-	8	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.  
 [2] Unused pins at V<sub>CC</sub> or GND.  
 [3] This is the bus hold overdrive current required to force the input to the opposite logic state.  
 [4] This parameter is valid for any V<sub>CC</sub> between 0 V and 1.2 V with a transition time of up to 10 ms.  
 From V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 3.3 V ± 0.3 V a transition time of 100 ms is permitted. This parameter is valid for T<sub>amb</sub> = +25 °C only.  
 [5] I<sub>CC</sub> with the outputs disabled is measured with outputs pulled to V<sub>CC</sub> or GND.  
 [6] This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.

## 10. Dynamic characteristics

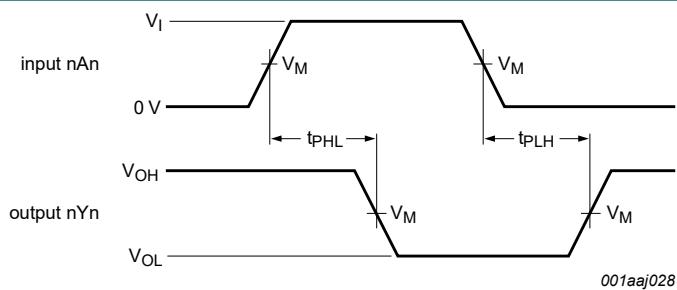
**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Fig. 7](#).

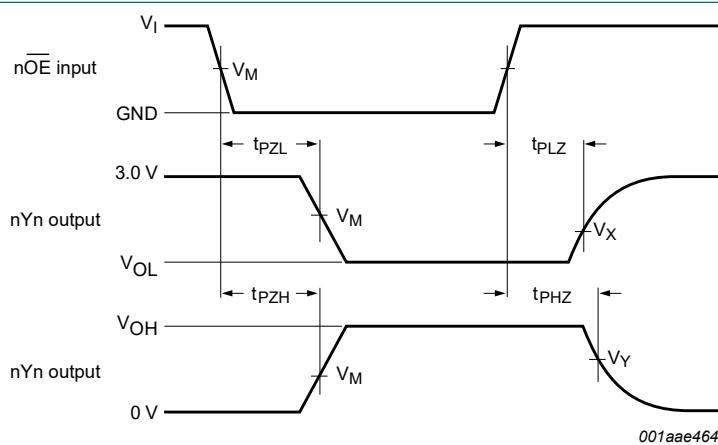
Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to nȲn; see <a href="#">Fig. 5</a>				
		V <sub>CC</sub> = 2.7 V	-	-	5.2	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	2.5	4.3	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to nȲn; see <a href="#">Fig. 5</a>				
		V <sub>CC</sub> = 2.7 V	-	-	5.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	2.5	4.3	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	nȲE to nȲn; see <a href="#">Fig. 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	6.3	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	3.7	5.2	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nȲE to nȲn; see <a href="#">Fig. 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	6.7	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.0	3.1	5.2	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	nȲE to nȲn; see <a href="#">Fig. 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	6.3	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	2.0	3.4	5.6	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	nȲE to nȲn; see <a href="#">Fig. 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	5.6	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V	1.6	3.2	5.1	ns

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 3.3 V.

### 10.1. Waveforms and test circuit



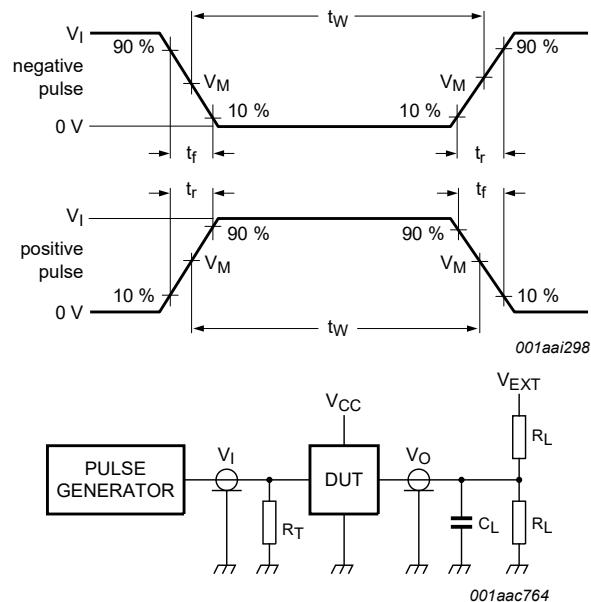
**Fig. 5. Input (nAn) to output (nYn) propagation delays**



**Fig. 6. 3-state enable and disable times**

**Table 8. Measurement points**

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

**Fig. 7. Test circuit for measuring switching times**

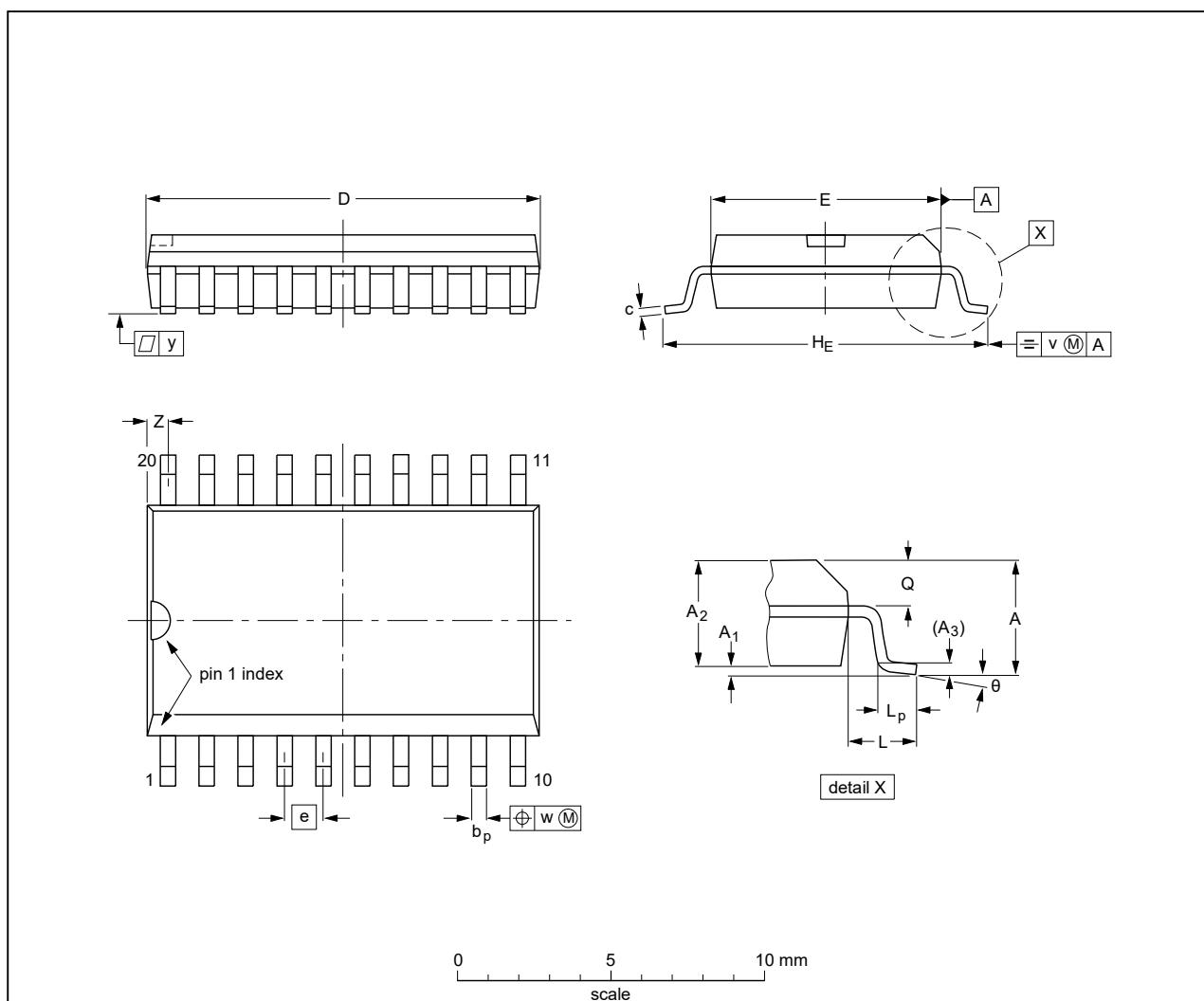
**Table 9. Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$R_L$	$C_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	500 $\Omega$	50 pF	GND	6 V	open

## 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

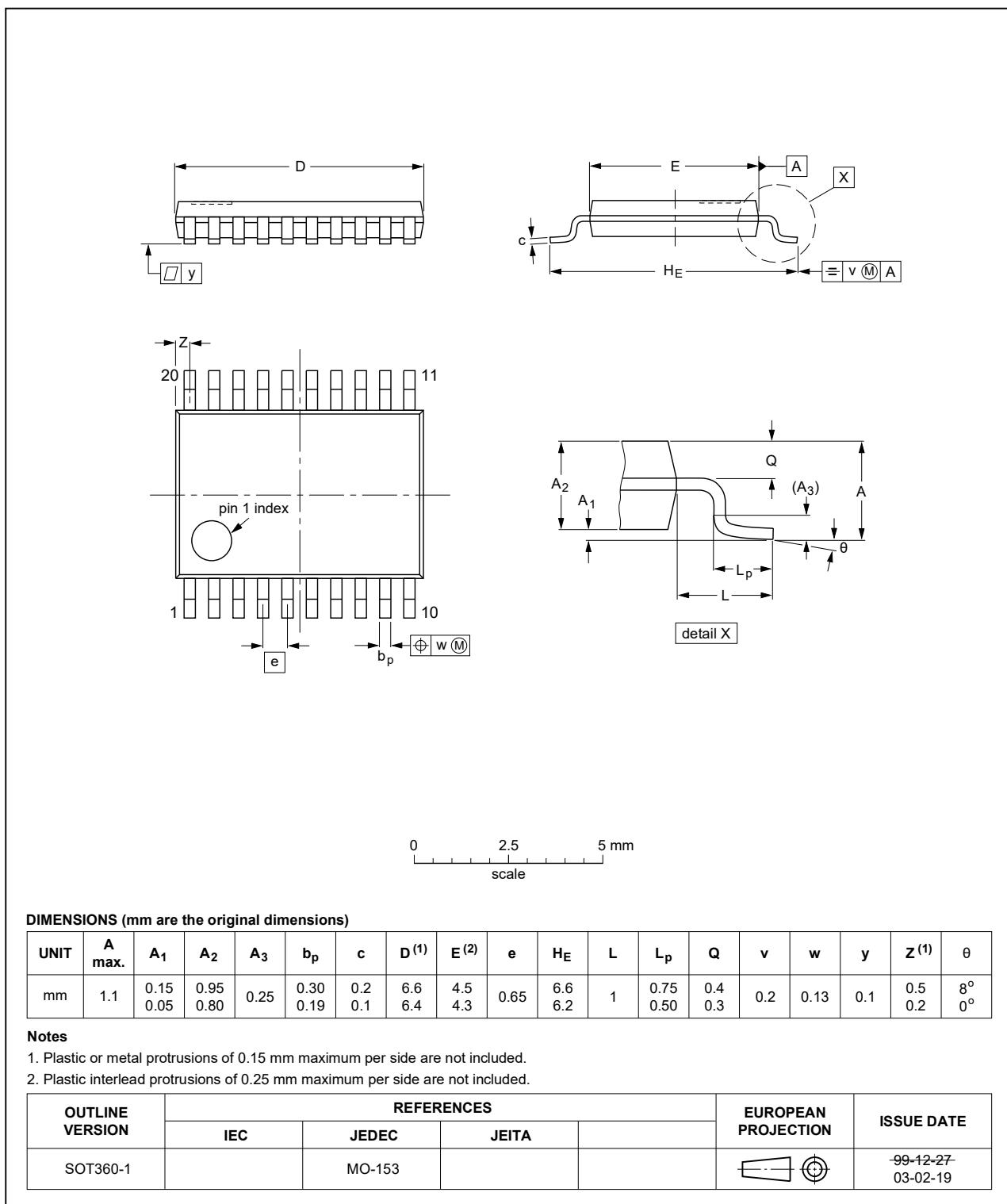


Fig. 9. Package outline SOT360-1 (TSSOP20)

## 12. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT240 v.4	20210728	Product data sheet	-	74LVT240 v.3
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVT240DB (SOT339-1/SSOP20) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation removed.</li> </ul>			
74LVT240 v.3	20170410	Product data sheet	-	74LVT240 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LVT240 v.2	19980219	Product specification	-	74LVT240 v.1
74LVT240 v.1	19940516	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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### 3.3 V Octal inverting buffer/line driver; 3-state

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